REMARKS

I. Overview

Claims 1-18 are pending in the present application. Claims 1, 4, 8 and 16 have been amended. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

The issues raised by the Examiner in the current Office Action dated May 6, 2008 ("the current Office Action") are as follows:

- Claims 1, 3-6, 8, 9, 11-13 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over U.S. Patent No. 5,829,038 to Merrel, et al. (hereinafter "Merrel"),and further in view of U.S. Patent No. 5,809,531 to Brabandt (hereinafter "Brabandt");
- Claim 2 has been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Merrel in view of Brabandt, and further in view of U.S. Patent No. 6,401,199 to Klein (hereinafter "Klein");
- Claims 7, 10 and 16-18 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Merrel in view of Brabandt, and further in view of "The Cache Memory Book by Jim Handy (hereinafter "Handy"); and
- Claims 14 and 15 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Merrel in view of Brabandt, and further in view of U.S. Patent No. 5,157,780 to Stewart, et al. (hereinafter "Stewart").

In response, Applicants respectfully traverse the outstanding claim rejections and requests reconsideration and withdrawal in light of the amendments and remarks presented herein.

II. Examiner Interview

Applicant's Attorney, Michael Fogarty (Reg. No. 42,541) and Examiner Michael Alsip conducted an Examiner Interview by telephone on June 24, 2008. Applicant's Attorney thanks the Examiner for his time during the interview. The parties discussed claims 1-18 and the Examiner's remarks in the current Office Action. Applicant's Attorney proposed amendments to independent claims clarifying that the claimed interface was outside the processor chip. Agreement was not reached. The Examiner indicated that he would need to review the proposed amendments and the cited references.

III. Amendments

Claims 1, 4 and 8 are amended herein. Applicant respectfully submits that no new matter is added by these amendments, which are supported in the original application at least at Figure 3 and 6.

IV. Claim Rejection – 35 U.S.C. § 103

Independent claim 1, as amended, recites:

> at least one processor chip including a processor unit and an internal data cache, and
>
> an interface external to the internal data cache and external to the processor chip, and configured to receive cache mirror data from the processor chip . . .

(emphasis added). Accordingly, the claimed "processor chip" includes both the processor unit and the internal data cache. The claimed "interface" is external to both the internal data cache and the processor chip.

The cited Merrell patent teaches a processor unit 10 coupled to a hierarchical cache system 15. There is no teaching in Merrell to split cache structure 15 into multiple components so that some parts are resident on the processor chip and other parts are external to the processor chip. Accordingly, as defined in claim 1, Merrell's processor unit 10 and cache system 15 would be included in the claimed "processor chip." The current Office Action cites cache levels L2-Ln as providing the claimed interface. Office Action at 2-3. However, cache levels L2-Ln are not "external to the processor chip" as required in claim 1. Moreover, Merrell's cache levels L2-Ln are integral to hierarchical cache structure 15 and, therefore, those levels are not "external to the internal data cache." Instead, cache level's L2-Ln form part of the internal data cache itself.

The Brabandt patent does not disclose an interface that is external to the internal data cache and the processor chip. Accordingly, the proposed combination of Merrell and Brabandt does not teach or suggest all of the elements of claim 1.

Claim 4 is directed to a method of operating a processing chip. The processing chip has "a processor, an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processing chip." Claim 4 recites:

> discarding the write instructions at an interface external to the processing chip so that cache mirror data is never written to external memory during operation of the processing chip, the external interface providing a connection between the processing chip and an address controller; . . .

(emphasis added). The Merrell patent discloses hierarchical cache structure 15, which is part of the claimed "processing chip" as defined in claim 4. Even if the cache structure 15 discarded write instructions as alleged in the current Office Action, the cache structure is not "external to the processing chip" as required in claim 4.

The Brabandt patent does not disclose discarding write instructions at an interface that is external to the processing chip. Accordingly, the proposed combination of Merrell and Brabandt does not teach or suggest all of the elements of claim 4.

Claim 8 recites:

> a processor chip including an internal processor coupled to an internal data cache;
> an external memory;
> an address decoder; and
> an interface external to the internal data cache and external to the processor chip, the interface coupled between the processor chip and the external memory and providing the only connection between the processor chip and the address decoder, . . .

(emphasis added). Accordingly, the claimed "processor chip" includes both the internal processor and the internal data cache. The claimed "interface" is external to both the internal data cache and the processor chip.

The Merrell patent teaches a processor unit 10 coupled to a hierarchical cache system 15. There is no teaching in Merrell to split cache structure 15 into multiple components so that some parts are resident on the processor chip and other parts are external to the processor chip. Accordingly, as defined in claim 1, Merrell's processor unit 10 and cache system 15 would be included in the claimed "processor chip." The current Office Action cites cache levels L2-Ln as providing the claimed interface. *See*, Office Action at 2-4. However, cache levels L2-Ln are not "external to the processor chip" as required in claim 8. Moreover, Merrell's cache levels L2-Ln are integral to hierarchical cache structure 15 and, therefore, those levels are not "external to the internal data cache." Instead, cache level's L2-Ln form part of the internal data cache itself.

Claim 8 further requires that the interface is provides the only connection between the processor chip and the address controller. The Merrell patent does not teach an address controller that is separate from the processing chip by the claimed interface.

The Brabandt patent does not disclose an interface that is external to the internal data cache and the processor chip. Accordingly, the proposed combination of Merrell and Brabandt does not teach or suggest all of the elements of claim 8.

Claim 16 is directed to a method of operating a data processing system having a plurality of integrated circuits. Each integrated circuit has a processor, an internal data cache, and a cache controller. Claim 16 recites:

> transmitting cache mirror data write instructions from a first cache controller of a first integrated circuit to an external memory interface, wherein the external memory interface is located outside the first integrated circuit, the external memory interface not operating as a data cache; . . .

(emphasis added). The Merrell patent teaches a processor unit 10 coupled to a hierarchical cache system 15. There is no teaching in Merrell to split cache structure 15 into multiple components so that some parts are resident on the integrated circuit and other parts are external to the integrated circuit. Accordingly, as defined in claim 16, Merrell's processor unit 10 and cache system 15 would be included in the claimed integrated circuits. The current Office Action cites cache levels L2-Ln as providing the claimed interface. Office Action at 10. However, cache levels L2-Ln are not a "external memory interface [] located outside the first integrated circuit" as required in claim 16.

The Brabandt patent does not disclose an external memory interface located outside the first integrated circuit.

The Handy reference teaches multiple level cache memories that are on-chip and off-chip. Handy does not teach an external memory interface that is not a cache memory, as required in claim 16.

Accordingly, the proposed combination of Merrell, Brabandt and Handy does not teach or suggest all of the elements of claim 16.

Claims 2, 3, 5-7, 9-15, 17 and 18 depend from independent claims 1, 8 and 16, respectively, and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

July 2, 2008
Date

/Michael J. Fogarty, III/
Michael J. Fogarty, III
Attorney for Applicants
Reg. No. 42,541

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218